Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A**
2. **G=NA**
3. **B**
4. **H=NB**
5. **C**
6. **I=NC**
7. **VSS**
8. **J=ND**
9. **D**
10. **K=NE**
11. **E**
12. **L=NF**
13. **F**
14. **VDD**

**DIE ID**

**2 1 14 13 12**

**5 6 7 8 9**

**11**

**10**

**3**

**4**

**CD40106B**

**.047”**

**.069”**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: CD40106B**

**APPROVED BY: DK DIE SIZE .048” X .069” DATE: 10/20/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: CD40106BH**

**DG 10.1.2**

#### Rev B, 7/19/02